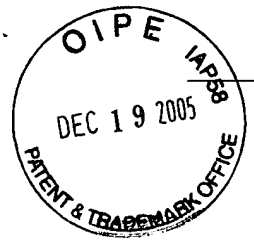
AFS
IFW



Please Direct All Correspondence to Customer Number **20995**

TRANSMITTAL LETTER
APPEAL BRIEF

Applicant	:	Agarwal et al.
App. No	:	10/687,086
Filed	:	October 16, 2003
For	:	BORON INCORPORATED DIFFUSION BARRIER MATERIAL
Examiner	:	Shouxiang Hu
Art Unit	:	2811

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

December 15, 2005
(Date)

Andrew N. Merickel, Reg. No. 53,317

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing in the above-identified application are the following enclosures:

(X) Appeal Brief in 17 pages.

FILING FEES:

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Appeal Brief	*41.20(b)(2)*	1402 ($500)		$500
1 Month Extension	*1.17(a)(1)*	1251 ($120)		$0
2 Month Extension	*1.17(a)(2)*	1252 ($450)		$0
3 Month Extension	*1.17(a)(3)*	1253 ($1,020)		$0
			TOTAL FEE DUE	$500

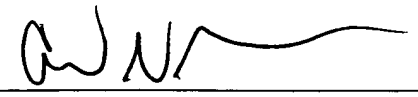
(X) A check in the amount of $500 is enclosed.

(X) Return prepaid postcard.

Docket No.	:	MICRON.095C1	**Customer No.: 20,995**
Application No.	:	10/687,086	
Filing Date	:	October 16, 2003	

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Dated: December 15, 2005



Andrew N. Merickel
Registration No. 53,317
Attorney of Record
Customer No. 20,995
(415) 954-4114

2212320_1
121505

Please Direct All Correspondence to Customer Number **20995**

APPEAL BRIEF

Applicant	:	Agarwal et al.
App. No	:	10/687,086
Filed	:	October 16, 2003
For	:	BORON INCORPORATED DIFFUSION BARRIER MATERIAL
Examiner	:	Shouxiang Hu
Art Unit	:	2811

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

December 15, 2005
(Date)

Andrew N. Merickel, Reg. No. 53,317

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the Notice of Appeal filed October 18, 2005, Applicants submit this Appeal Brief.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party of interest in the present application is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 C.F.R. § 41.37(c)(2), Appellants hereby notify the Board of Patent Appeals that Appellants, the Appellants' Legal Representative, and the Assignee do not know of any appeals or interferences that will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-10 and 23-33 are currently pending in the application, and are attached hereto as an appendix. All of the pending claims were finally rejected by the Examiner and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

Appellants amended Claim 23 in response to the first Office Action. In addition, Appellants canceled Claims 11-22 subsequent to the Final Office Action. No claims have been amended subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to an integrated circuit structure, and more particularly, to an integrated circuit structure having a diffusion barrier layer for preventing fluorine atom diffusion.

One aspect of the present invention is an integrated circuit structure 10 comprising: a gate oxide layer 14; a titanium boronitride barrier layer 30 above at least a portion of the gate oxide layer 14; a polysilicon layer 20 above at least a portion of the titanium boronitride layer 30; and a conductive layer 40 above at least a portion of the polysilicon layer 20, wherein the conductive layer 40 has at least some fluorine atoms or ions therein, and wherein the titanium boronitride barrier layer 30 inhibits diffusion of the fluorine atoms or ions from the conductive layer 40 into the gate oxide layer 14. Reference numbers are to the present application unless indicated otherwise. Paragraph [0048] and Figure 6 illustrate an example of the claimed integrated circuit structure.

Another aspect of the present invention includes a gate electrode 50 comprising: a dielectric layer 14; a diffusion barrier layer 30 comprising titanium boronitride formed over at least a portion of the dielectric layer 14; a polysilicon layer 20 formed over at least a portion of the diffusion barrier layer 30; and a conductive layer 40 formed over at least a portion of the polysilicon layer 20, wherein the conductive layer 40 has at least some fluorine atoms or ions therein, and wherein the diffusion barrier layer 30 inhibits fluorine diffusion from the conductive layer 40 into the dielectric layer 14. Reference numbers are to the present application unless indicated otherwise. Paragraph [0048] and Figure 6 illustrate an example of the claimed gate electrode.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A) Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being obvious over European patent No. 854505 A2 to Lu et al. ("Lu") in view of U.S. Patent No. 5,364,803 to Lur et al. ("Lur").

B) Claims 23-33 were rejected under 35 U.S.C. § 103(a) as being obvious over Lu in view of Lur.

VII. ARGUMENT

Discussion of the Lu Reference Relied Upon by the Examiner

Appellants and the Examiner disagree on the teachings of Lu. In the Final Office Action of July 19, 2005, the Examiner indicated that Lu discloses a gate structure in an integrated circuit structure (Fig. 3; also see page 4, line 36-37), comprising: a TiN_xB_y barrier layer overlying a dielectric layer (5; a gate oxide) and underlying a conductive layer comprising tungsten in a gate electrode (14). The Examiner also pointed out that Lu further discloses that the gate electrode (14) can be a poly-tungsten stack for lowering the sheet resistance of the gate electrode structure (see page 4, lines 30-31). The Examiner noted that the term "poly-tungsten stack" commonly means a polysilicon-tungsten stack with a polysilicon layer underlying a tungsten or tungsten silicide layer. In addition, the Examiner found that Lu further discloses that the TiN_xB_y layer can be between a gate insulator (gate dielectric or oxide layer) and a poly-tungsten stack with polysilicon underlying tungsten.

Appellants disagree to the Examiner's finding that Lu discloses that the TiN_xB_y layer can be between the gate insulator and the poly-tungsten stack with polysilicon underlying tungsten. Lu neither discloses nor teaches such a structure. Rather, the Examiner confuses two separate embodiments disclosed in the same paragraph of Lu: (1) a first embodiment with a TiN_xB_y layer between polysilicon and tungsten layers; and (2) a second embodiment with a TiN_xB_y layer between gate oxide and tungsten layers without any polysilicon. Appendix A, attached hereto, clarifies the differences between these two disclosed embodiments of Lu and the claimed structure.

1) First Embodiment of Lu

The first embodiment of Lu only indicates that a TiN_xB_y layer can be between polysilicon and tungsten layers. Lu provides the first embodiment as follows:

> Figure 3 is a cross-sectional view of transistors which utilize the described embodiments so as to form a portion of gate structure 14. Gate structure 14 can be formed using polysilicon (preferably doped), silicided polysilicon, or a metal. However, use of a stack (preferably a poly-metal stack – more preferably a poly-tungsten stack) will lower the sheet resistance of the gate structure and therefore the device would have a reduced RC constant (hence, higher performance). However, a diffusion barrier is needed to prevent a reaction between the tungsten and the poly. In addition, an adhesion promoter is needed in a tungsten-based gate structure so as to better adhere the tungsten layer to the gate insulator 5. More specifically, the TiN, $TiSi_xN_y$, or TiN_xB_y layers, which are formed using the described embodiments, would be used between the polysilicon portion of gate structure 14 and the overlying tungsten

> portion of gate 14 or it would be used between gate insulator 5 (preferably an oxide, a nitride, or a combination thereof) and gate structure 14 which is preferably comprised of tungsten. Page 4 at lines 28-37 (emphasis added).

In the above underlined sentences, Lu discloses that the TiN_xB_y layer can be positioned as a diffusion barrier between the polysilicon and tungsten layers, but not anywhere else.

In addition, the first embodiment of Lu does not teach or suggest the claimed position of the TiN_xB_y layer between the gate insulator and the polysilicon layer. According to the above disclosure of Lu, the "diffusion barrier" is used to prevent a reaction between the tungsten and the polysilicon layers. The diffusion barrier functions as intended only between the tungsten and the polysilicon layers, not anywhere else. If the TiN_xB_y layer were between the gate insulator and the polysilicon layer, as claimed, it would not function as a diffusion barrier to prevent a reaction between the tungsten and the poly layers. Therefore, the above disclosure of Lu does not teach or suggest having the claimed position for a TiN_xB_y layer, between a gate insulator and a polysilicon layer.

2) Second Embodiment of Lu

In the second embodiment, Lu only indicates that a TiN_xB_y layer would be used between a gate insulator and a tungsten-only layer, without any polysilicon. Lu, in pertinent part, discloses:

> Figure 3 is a cross-sectional view of transistors which utilize the described embodiments so as to form a portion of gate structure 14. Gate structure 14 can be formed using polysilicon (preferably doped), silicided polysilicon, or a metal. However, use of a stack (preferably a poly-metal stack – more preferably a poly-tungsten stack) will lower the sheet resistance of the gate

> structure and therefore the device would have a reduced RC constant (hence, higher performance). However, a diffusion barrier is needed to prevent a reaction between the tungsten and the poly. In addition, an adhesion promoter is needed in a tungsten-based gate structure so as to better adhere the tungsten layer to the gate insulator 5. More specifically, the TiN, $TiSi_xN_y$, or TiN_xB_y layers, which are formed using the described embodiments, would be used between the polysilicon portion of gate structure 14 and the overlying tungsten portion of gate 14 or it would be used between gate insulator 5 (preferably an oxide, a nitride, or a combination thereof) and gate structure 14 which is preferably comprised of tungsten. Page 4 at lines 28-37 (emphasis added).

In the above underlined sentences, Lu only discloses that a TiN_xB_y layer would be used directly between a gate insulator and tungsten. Lu's second embodiment relates to a gate insulator/TiN_xB_y layer/tungsten stack, with no polysilicon.

In addition, the second embodiment of Lu neither teaches nor suggests the claimed position of the TiN_xB_y layer. The function of the TiN_xB_y layer as an adhesion promoter between gate insulator and tungsten provides no teaching or suggestion that the TiN_xB_y layer can be between a gate insulator and a polysilicon layer. Indeed, this asserted function of Lu's second gate stack embodiment has no application to use of polysilicon between tungsten and the gate insulator; it is only in the absence of polysilicon that Lu suggests a TiN_xB_y layer can or should directly overlie the gate insulator. Thus, positioning the TiNxBy layer between a gate insulator and a polysilicon layer, as claimed in the present application, is inconsistent with Lu's asserted function of the layer as an adhesion promoter between gate insulator and tungsten.

As discussed above, Lu fails to disclose or suggest that a TiN_xB_y layer can be between a gate insulator and a polysilicon layer. In addition, the disclosed functions of the TiN_xB_y layer as a diffusion barrier to prevent poly-tungsten interactions (the first embodiment) or an adhesion promoter between gate insulator and tungsten (the second embodiment) neither teaches nor suggests having a TiN_xB_y layer between a gate insulator and polysilicon. Therefore, the Examiner's finding that Lu discloses that the TiN_xB_y barrier layer can be between the gate insulator and the poly-tungsten stack lacks a factual basis and confuses the first Lu embodiment (which employs a barrier between tungsten and polysilicon) and the second Lu embodiment (which employs an adhesion promoter between gate insulator and tungsten).

No *Prima Facie* Case of Obviousness

A) Claims 1-10 are not obvious from Lu in view of Lur

The Examiner rejected Claim 1-10 as being obvious from Lu in view of Lur. However, the Examiner has not established a *prima facie* case of obviousness. The Patent and Trademark Office has the burden under section 103 to establish a *prima facie* case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-87 (Fed. Cir. 1984). To establish a *prima facie* case of obviousness, three basic criteria must be met: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143 (emphasis added).

1) Failure to Provide All Claim Limitations

Lu and Lur, either alone or combined, do not teach or suggest all the claim limitations of Claim 1. Claim 1 is directed to an integrated circuit structure having a titanium boronitride diffusion barrier layer between a gate oxide layer and a polysilicon layer, the diffusion barrier layer inhibiting diffusion of fluorine atoms from the conductive layer into the gate oxide layer.

First, neither Lu nor Lur teaches or suggests that a TiN_xB_y layer can be in the claimed position between a gate oxide layer and a polysilicon layer. Initially, note that Lu is cited for its teachings of TiN_xB_y diffusion barriers and their positions in a gate stack. Lur is a secondary reference for supplying the existence of fluorine in a gate layer, but teaches nothing about TiN_xB_y diffusion barriers or their positions.

Neither of the asserted references teaches or suggests the claimed position for a TiN_xB_y layer, i.e., between a gate insulator and a polysilicon layer. The Examiner rejected Claim 1 based on the finding that Lu discloses that a TiN_xB_y layer can be between a gate insulator and a poly-tungsten stack with poly underlying tungsten. As explained above, however, the Examiner's finding lacks a factual basis. Lu only teaches or suggests that a TiN_xB_y layer can be (1) directly between a gate insulator and a tungsten layer or (2) between a polysilicon layer and a tungsten layer. In addition, the secondary reference, Lur, only teaches or suggests that a diffusion barrier layer can be between polysilicon and a tungsten silicide layer and fails to teach anything about TiN_xB_y layers. The references therefore, either alone or in combination, fail to teach or suggest the position of the TiN_xB_y layer of Claim 1.

Second, neither Lu nor Lur teaches or suggests that a "TiN_xB_y" layer can or should be configured to function as a barrier to fluorine diffusion. Lu discloses that a TiN_xB_y layer can be used either as an adhesion promoter or as a poly-tungsten diffusion barrier. In addition, Lu provides that TiN_xB_y can be used as a diffusion barrier to prevent diffusion/reaction of the via/contact/trench metals with silicon, silicides, or dielectric materials. *See* Lu, page 4, lines 6-10. However, there is no mention of a barrier against fluorine diffusion in Lu. In addition, Lur only discloses that TiN_x, TiW or TaN can be used as a fluorine diffusion barrier. Therefore, neither Lu nor Lur teaches or suggests that a TiN_xB_y layer can be a "fluorine" diffusion barrier.

As discussed above, neither Lu nor Lur provides the position or the function of the TiN_xB_y layer which are essential limitations of Claim 1. Therefore, Lu and Lur, either alone or in combination, do not teach or suggest all the claim limitations of Claim 1.

2) No Suggestion or Motivation

Neither Lu nor Lur provides any suggestion or motivation to modify the references or to combine their teachings to achieve the integrated circuit structure of Claim 1. The references provide no suggestion or motivation for the claimed position or function of the TiN_xB_y layer.

Lu and Lur, either alone or combined, do not provide suggestion or motivation for the claimed position of the TiN_xB_y layer. As discussed above with respect to the functions of the TiN_xB_y layer in Lu, Lu does not suggest having a TiN_xB_y layer between a gate oxide layer and a polysilicon layer. The secondary reference, Lur, does not cure this deficiency, as Lur does not suggest positioning any

sort of diffusion barrier between a gate oxide layer and a polysilicon layer, much less a TiN_xB_y layer.

In addition, the references provide no suggestion or motivation for configuring a TiN_xB_y layer as a fluorine diffusion barrier layer. Lur provides no suggestion or motivation to modify Lu to use a TiN_xB_y layer as a "fluorine" diffusion barrier. Lu discloses that TiN_xB_y can be used as either an adhesion promoter between tungsten and oxide or a diffusion barrier between poly and tungsten. Lur does not mention TiN_xB_y at all. Lur only discloses that TiN_x, TiW or TaN are preferred "fluorine" diffusion barrier materials. Given no disclosure of Lur regarding TiN_xB_y, a skilled artisan would not be motivated to use TiN_xB_y of Lu as a "fluorine" diffusion barrier.

As discussed above, at least two of the requirements for a *prima facie* case of obviousness have not been satisfied. Thus, Claim 1 is not obvious over Lu in view of Lur. Therefore, Claims 2-10, while depend from Claim 1 and contain all of the features thereof in addition to further distinguishing features, are not obvious either. Accordingly, Appellants submit that the Examiner's rejection of Claims 1-10 should be reversed by the Board.

B) Claims 23-33 are not obvious from Lu in view of Lur

Claim 23 is directed to a gate electrode comprising a dielectric layer; a TiN_xB_y diffusion barrier layer; a polysilicon layer; and a conductive layer, the diffusion barrier layer inhibiting fluorine diffusion from the conductive layer into the dielectric layer. The position and function of the TiN_xB_y layer in Claim 23 are identical to those of Claim 1. Therefore, as discussed above with respect to Claim 1, Claim 23 is not obvious from Lu in view of Lur. Therefore, Claims 24-33,

while depend from Claim 23, are not obvious either. Accordingly, Appellants submit that the Examiner's rejection of Claims 23-33 should be reversed by the Board.

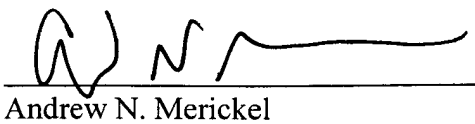
SUMMARY

1. The claimed position of the TiN_xB_y layer (see APPENDIX A, Figure (c)) is not disclosed in Lu (see APPENDIX A, Figures (a) and (b)). Contrary to the Examiner's assertions, Lu fails to teach a TiN_xB_y layer between a gate insulator and a polysilicon layer.

2. No motive for using the TiN_xB_y layer as a fluorine diffusion barrier is provided by Lu. Lu only discloses a TiN_xB_y layer as a diffusion barrier between polysilicon and tungsten or as an adhesion promoter between tungsten and gate oxide.

3. Lur does not cure the deficiencies of Lu. Lur discloses nothing about TiN_xB_y or the claimed position for a fluorine diffusion layer.

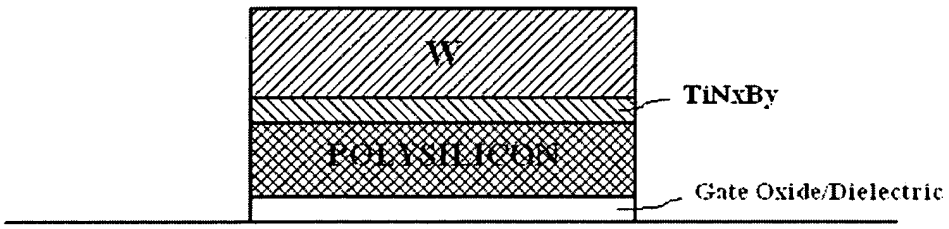
In view of the foregoing, Appellants respectfully submit that the final rejections depend upon factual misunderstandings of the prior art teachings, in particular on the mistaken belief that Lu teaches use of a TiN_xB_y layer between a gate oxide and polysilicon. As Lu neither teaches the claimed position for a titanium boronitride barrier layer, nor provides any suggestion or motivation for this position, and Lur does not make up for this critical deficiency, Appellants respectfully request reversal of the final rejections.



Andrew N. Merickel
Registration No. 53,317
Attorney of Record
Customer No. 20,995
(415) 954-4114

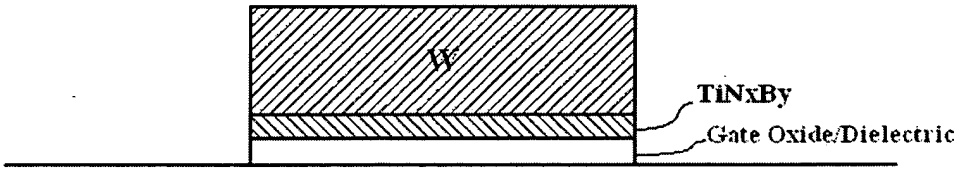
VIII. APPENDIX A

(a)



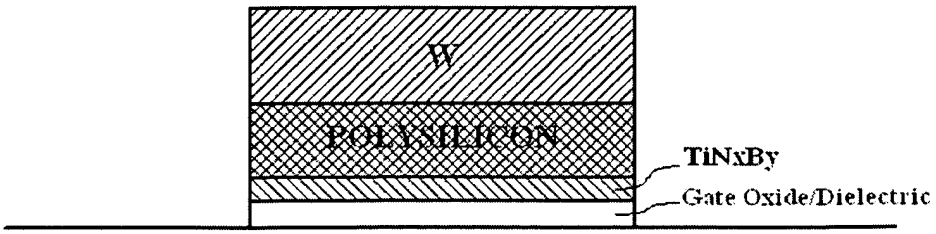
Lu Embodiment 1

(b)



Lu Embodiment 2

(c)



Claims

IX. CLAIMS APPENDIX

1. An integrated circuit structure comprising:

a gate oxide layer;

a titanium boronitride barrier layer above at least a portion of the gate oxide layer;

a polysilicon layer above at least a portion of the titanium boronitride layer; and

a conductive layer above at least a portion of the polysilicon layer, wherein the conductive layer has at least some fluorine atoms or ions therein, and wherein the titanium boronitride barrier layer inhibits diffusion of the fluorine atoms or ions from the conductive layer into the gate oxide layer.

2. The integrated circuit structure of Claim 1 wherein the gate oxide layer has a thickness of about 30 angstroms to about 200 angstroms.

3. The integrated circuit structure of Claim 1 wherein the polysilicon layer has a thickness of about 300 angstroms to about 1,500 angstroms.

4. The integrated circuit structure of Claim 1 wherein the titanium boronitride layer has a thickness of about 50 angstroms to about 500 angstroms.

5. The integrated circuit structure of Claim 1 wherein the conductive layer comprises tungsten.

6. The integrated circuit structure of Claim 1 wherein the conductive layer comprises tungsten silicide.

7. The integrated circuit structure of Claim 1 wherein the conductive layer has a thickness of about 200 angstroms to about 4,000 angstroms.

8. The integrated circuit structure of Claim 1 further comprising a semiconductor substrate.

9. The integrated circuit structure of Claim 8 wherein the semiconductor substrate comprises an intrinsically doped monocrystalline silicon wafer.

10. The integrated circuit structure of Claim 8 wherein the semiconductor substrate comprises an operable portion of a transistor array in a memory device.

11-22. (Canceled)

23. A gate electrode comprising:

a dielectric layer;

a diffusion barrier layer comprising titanium boronitride formed over at least a portion of the dielectric layer;

a polysilicon layer formed over at least a portion of the diffusion barrier layer; and

a conductive layer formed over at least a portion of the polysilicon layer, wherein the conductive layer has at least some fluorine atoms or ions therein, and wherein the diffusion barrier layer inhibits fluorine diffusion from the conductive layer into the dielectric layer.

24. The gate electrode of Claim 23 wherein the dielectric layer is a gate oxide layer.

25. The gate electrode of Claim 23 wherein the gate oxide layer has a thickness of about 30 angstroms to about 200 angstroms.

26. The gate electrode of Claim 23 wherein the polysilicon layer has a thickness of about 300 angstroms to about 1,500 angstroms.

27. The gate electrode of Claim 23 wherein the titanium boronitride has a thickness of about 50 angstroms to about 500 angstroms.

28. The gate electrode of Claim 23 wherein the conductive layer comprises tungsten.

29. The gate electrode of Claim 23 wherein the conductive layer comprises tungsten silicide.

30. The gate electrode of Claim 23 wherein the conductive layer has a thickness of about 200 angstroms to about 4,000 angstroms.

31. The gate electrode of Claim 23 further comprising a semiconductor substrate.

32. The gate electrode of Claim 31 wherein the semiconductor substrate comprises an intrinsically doped monocrystalline silicon wafer.

33. The gate electrode of Claim 31 wherein the semiconductor substrate comprises an operable portion of a transistor array in a memory device.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.

2211986_1
121505